In The Claims:

Claims 1-8 (canceled)

Claim 9. (original) A low temperature poly-silicon thin film transistor (LTPS TFT), comprising:

a poly-silicon layer, deposited on a substrate, wherein the height/width ratio of a plurality of mounds on a surface of the poly-silicon layer is less than 0.2, and the poly-silicon layer comprises a source, a drain, and a channel that is deposited in between the source and the drain;

a gate isolation layer, deposited on the substrate, and covering the poly-silicon layer;

a gate, correspondingly deposited on the gate isolation layer that is deposited above the channel;

a dielectric layer, deposited on the gate isolation layer, and covering the gate;

a source metal layer, deposited on a surface of the dielectric layer and in the dielectric layer and the gate isolation layer wherein the source metal layer is electrically connected to the source; and

a drain metal layer, deposited on the surface of the dielectric layer and in the dielectric layer and the gate isolation layer wherein the drain metal layer is electrically connected to the drain.

Claim 10. (currently amended) The low temperature poly-silicon thin film transistor of claim 9, further comprising ~~a step of depositing~~ a buffer layer in between the substrate and the ~~amorphous~~ poly-silicon layer.